



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,096	07/02/2003	Joo-Won Lee	SAM-0429	3427
7590	05/09/2006			EXAMINER NADAV, ORI
Anthony P. Onello, Jr. MILLS & ONELLO LLP Suite 605 Eleven Beacon Street Boston, MA 02108			ART UNIT 2811	PAPER NUMBER

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/612,096	LEE ET AL.
Examiner	Art Unit	
Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 09 March 2006.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-9 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-9 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 recites a first line unit which functions as an electrode line. That is, the first line unit must be a conductive element. There is no support in the specification for an insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, as recited in claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ejiri (6,770,974) in view of Applicant Admitted Prior Art (AAPA).

Ejiri teaches in figure 13 and related text an electrode line structure of a semiconductor device comprising:

a semiconductor substrate 10, and

an electrode line 18 formed on the semiconductor substrate, the electrode line having an inclined outer end in the long axis direction;

wherein the electrode line comprise one of word line and bit line of the semiconductor device, and wherein the electrode line includes a first line unit 18b, which substantially functions as an electrode line, a second line unit 18c, which includes the inclined outer end in the long axis direction and which is separated from the first line unit by a predetermined distance, and an insulating plug 24, which is interposed between the first line unit and the second line unit and electrically insulates the first line unit from the second line unit, the insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit.

Ejiri does not disclose that the device comprises plurality of electrode lines being one of word lines and bit lines.

AAPA teaches in figure 1B plurality of electrode lines 20 having inclined ends and being one of word lines and bit lines.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use plurality of electrode lines in Ejiri's device in order to use the

device in a practical application which includes plurality of electrode lines, and in order to improve the characteristics of a device in an application which requires one of word lines and bit lines.

The combination is motivated by the teachings of AAPA, which point out the need to prevent the electrode of the device from being partially removed during the etching process (pages 1-3), and by the teachings of Ejiri who points out the advantages of preventing the electrode of the device from being damaged during the etching process (e.g. column 6, lines 1-6).

Regarding the claimed limitations of an insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, these features are inherent in Ejiri's device, because a plug is considered as an element formed in a via or in a space between two other elements. Therefore, the insulating material formed over the upper surface of the first line unit and the second line unit in Ejiri's device, cannot be considered as a "plug". Therefore, Ejiri teaches an insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, as claimed.

Furthermore, applicant argues that the insulating plug must have an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, because the first line unit and the second line unit are considered to be the conductive material together with the insulating material formed over the conductive material. Clearly, Ejiri teaches the insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper

surface of the second line unit, if the first line unit and the second line unit are considered to be the conductive material together with the insulating material formed over the conductive material.

Regarding claims 2 and 3, Ejiri does not state that the length of the electrode lines greater than a length of conventional electrode lines by a predetermined length and the insulating plug is formed at a predetermined position of each of the electrode lines such that the first line unit has the ordinary length. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the length of the electrode lines greater than a length of conventional electrode lines by a predetermined length and the insulating plug is formed at a predetermined position of each of the electrode lines such that the first line unit has the ordinary length in Ejiri's device in order to use the device in an application which requires specific electrode length.

Regarding claim 4, Ejiri teaches in figure 13 and related text the length of the second line unit is greater than a width of the electrode lines and less than the ordinary length.

Regarding claims 5 and 8, AAPA teaches the first line unit and the second line unit each comprise a conductive layer and a hard mask layer, respectively, a spacer is formed on the inclined end in the long axis direction of the second line unit. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the first line unit and the second line unit each with a conductive layer and a hard mask

layer, respectively, and to use a spacer on the inclined end in the long axis direction of the second line unit, in Ejiri's device in order to form the electrode lines in a conventional method using hard mask, in order to provide better protection to the electrode lines, respectively.

Regarding claims 6 and 7, Ejiri teaches a conductive layer comprises a material containing tungsten. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use electrode lines comprising a material containing tungsten and a hard mask layer comprises a silicon nitride layer or a silicon oxynitride layer in Ejiri's device in order to provide better conductivity and insulation to the electrode lines.

Regarding claim 9, Ejiri does not teach forming the insulating plug of a material of which the spacer is formed. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the insulating plug of a material of which the spacer is formed in Ejiri's device in order to simplify the processing steps of making the device.

Response to Arguments

Applicant argues that Ejiri does not teach an insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, as recited in claim 1.

Regarding the claimed limitations of an insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, these features are inherent in Ejiri's device, because a plug is considered as an element formed in a via or in a space between two other elements. Therefore, the insulating material formed over the upper surface of the first line unit and the second line unit in Ejiri's device, cannot be considered as a "plug". Therefore, Ejiri teaches an insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, as claimed.

Furthermore, applicant argues that the insulating plug must have an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, because the first line unit and the second line unit are considered to be the conductive material together with the insulating material formed over the conductive material. Clearly, Ejiri teaches the insulating plug having an upper surface that is at a same level as an upper surface of the first line unit and an upper surface of the second line unit, if the first line unit and the second line unit are considered to be the conductive material together with the insulating material formed over the conductive material.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660.

The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



O.N.
5/3/06

ORI NADA
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800